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Remarks

By this amendment claims 7 through 20 have been cancelled and claims 1 and 8 have been amended. Claims 1 through 16 are pending and reconsideration thereof is requested.

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In the Specification

The disclosure was objected to because of the following informalities: In Line 10 of Paragraph 32, numbers in scientific notation should be expressed as powers of 10 instead of "E" format. By this amendment an appropriate correction has been made. Accordingly, the Examiner is respectfully requested to remove the objection to the Specification.

Claim Objections

The Examiner objected to the claims because a claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. The Examiner mentioned it should be kept in mind that a dependent claim may refer to any preceding independent claim. The Applicants have amended Claim 8 to depend on Claim 7 to properly adjust the sequence of the claims in accordance with MPEP§608.01(n). Accordingly, the Examiner is respectfully requested to remove this objection to the claims.

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Claim Rejections - 35 U.S.C.§112

The Examiner rejected claims 1 to 15 under 35 U.S.C.§ 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner indicated that in Claim 1, the phrase "at least approximately" is indefinite since it is unclear what the metes and bounds of the limitation are. The Applicants have amended Claim 1 to overcome this rejection.

The Examiner indicated it is unclear to which of the transfer devices Claim 8 is referring to (i.e., "said transfer device") because Claim 1 describes first and second transfer devices. The Applicants have amended Claim 8 to specify a particular transfer device to overcome this rejection.

Based on the foregoing, it is respectfully submitted that Claims 1 to 15 are now allowable under 35 U.S.C.§ 112, second paragraph.

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Claim Rejections - 35 U.S.C. § 103

The Examiner rejected Claims 1,2,5,8 and 9 under 35 U.S.C.§ 103(a) as being unpatentable over Ota et al (U.S. Patent No. 5,329,479) and Iizuka et al (U.S. Patent No. 4,641,165). The Examiner correctly points out that Ota et al show the first and second transfer devices and a differential storage node and that Iizuka et al. show diffused electrodes. The Applicants respectfully believe that the references do not show, or suggest, the present invention. Further, Iizuka et al. do not teach a differential capacitance at least 5 times the inherent capacitances since Iizuka does not incorporate a differential capacitor. It is not clear as to what would serve as a differential node in Iizuka et al., namely the substrate, brings with it a very large capacitance to the storage node. No motivation appears in the cited references to produce the claimed invention, consider if one were to re-wire the capacitor of Iizuka et al. in a differential manner, it would not present at least 5 times the inherent capacitance without further invention. The work of Ota et al. also fails to teach how the capacitor of Iizuka et al. could be re-wired to accomplish this requirement. Thus, the works of Ota et al. and Iizuka et al. taken together require further invention to identify a low-capacitance means of wiring the second capacitor node of Iizuka et al. differentially. Furthermore, neither work identifies the use of fully-depleted transfer devices which are the subject of Claims 1,2,5,8 and 9 in order to enable the capacitance goals recited therein.

Based on the foregoing, it is submitted that Claims 1,2,5,8 and 9 are not obvious under 35 U.S.C.§103(a).

The Examiner rejected claims 3 and 4 under 35 U.S.C. 103(a) as being unpatentable over Ota et al. and Iizuka et al., as applied to Claim 1 above, and further in view of Tashiro (U.S. Patent No. 5,241,211).

The Examiner indicated that Ota et al. and Iizuka et al. show most aspects of the instant invention except for the SOI substrate. Tashiro teaches (e.g. Column 1, Lines 14 to 23) to use SOI substrates to reduce parasitic capacitances. The Examiner believes that it would have been obvious to a person of ordinary skill in the art at the time of invention to use an SOI substrate as taught by Tashiro in the device of Ota et al. and Iizuka et al. to reduce parasitic capacitances.

The Applicants point out that Iizuka et al. and Ota et al. do not suggest the invention of Claim 1. Nor does Tashiro teach or suggest the use of an SOI substrate for a U-groove structure. Tashiro does not address the issues of providing low intrinsic (isolation) capacitance for a differential capacitor. Thus claims 3 and 4 are not made obvious by Tashiro, even taken with Ota et al. and Iizuka et al.

Based on the foregoing, it is submitted that claims 3 and 4 are not obvious under 35 U.S.C.§ 103(a).

The Examiner rejected claims 6,7,and 10 to 16 under 35 U.S.C.§103(a) as being unpatentable over Ota et al. and Iizuka et al., as applied to Claim 1 above, and further in view of Choi et al. (DRC 2000).

The Examiner indicated that Ota et al. and Iizuka et al. show most aspects of the instant invention except for the features of the transfer devices and the storage capacitor disposed on rails of semiconductor material. Choi et al. teach (e.g. Figure 1) to form semiconductor devices using semiconductor rails to reduce parasitic capacitance and resistance. The Examiner believes it would have been obvious to a person or ordinary skill in the art at the time of invention to form semiconductor devices using semiconductor rails as taught by Choi et al. in the device of Ota et al. and Iizuka et al. to reduce parasitic capacitance and resistance.

The Applicants point out again that Iizuka et al. and Ota et al. do not suggest the invention of Claim 1. Nor does Choi et al. teach or suggest the use of ultra-thin-body SOI to form and FET. They do not contribute to the use of "rails" nor differential capacitor configurations. They further teach away from rails in that they describe planar thin silicon with the body plane parallel

to the wafer substrate, in contrast to our invention where the body planes are explicitly perpendicular to the wafer substrate in order to provide low parasitic capacitance to the substrate.

Based on the foregoing, it is submitted that Claims 6, 7, and 10 to 16 are not obvious under 35 U.S.C.§103(a).

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

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